Appl. No. 10/695,976
Amdt. dated July 13, 2006
Reply to Office Action of June 7, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1. (currently amended) A method comprising:

receiving a serial stream of data bits;

deserializing the serial stream of data bits into parallel bits;

inputting the parallel bits into a content addressable memory and a first register;

inputting an output of the first register into a second register;

inputting outputs of the first and second registers to the content addressable memory;

providing a bus configured to receive the parallel bits and output of the first register, wherein the data lines forming the bus are grouped into a plurality of overlapping subsets of the bus that each contain at least one common data line;

providing the parallel bits and the output of the first register in a plurality of parallel bit outputs ~~formats~~ onto the bus; and

selecting one of the subsets and associated parallel bit outputs ~~formats to output~~ based on match flag outputs from the content addressable memory, wherein the match flag outputs are generated in response to the inputs to the content addressable memory.

Claim 2. (currently amended) The method of claim 1 wherein the plurality of parallel bits and the output of the first register ~~output formats~~ are input to a plurality of tristate driver circuits, and wherein selecting one of the subsets and the associated parallel bit outputs ~~formats to output~~ comprises:

enabling one of the tristate driver circuits to output the parallel bits and the output of the first register ~~output format~~ associated with that tristate driver ~~circuits~~ circuit to an output bus, and disabling other ones of the tristate driver circuits coupled to the output bus.

Claim 3. (original) The method of claim 1 wherein there are eight parallel bits.

Claim 4. (original) The method of claim 1 wherein the first and second registers are two stages of a shift register.

Claim 5. (original) The method of claim 1 wherein a depth of the content addressable memory comprises at least one row for each of the parallel bits.

Claim 6. (original) The method of claim 1 wherein the inputs to the content addressable memory are provided by way of parallel transfer.

Claim 7. (original) The method of claim 6 wherein a width of the parallel bits inputting the content addressable memory is at least a number of parallel bits output from the deserializer plus a length of a pattern to be detected using the content addressable memory minus 1.

Claim 8. (currently amended) A circuit comprising:

a deserializer circuit coupled to receive serial data input and outputting a first parallel data ~~of~~ output, wherein the deserializer circuit outputs the first parallel data onto a bus that is configured with overlapping subsets of the bus, wherein the subsets include at least one common data line;

a shift register coupled to the first parallel data output; and

a content addressable memory, coupled to the shift register to receive the first parallel data output in parallel.

Claim 9. (currently amended) The circuit of claim 8 further comprising:

a plurality of second parallel data outputs ~~formats~~ based on the first parallel data output, wherein each of second parallel data outputs are associated with a respective one of the subsets; and

a plurality of tristate buffer circuits, one coupled to each of the subsets of the bus ~~parallel data output formats~~.

Claim 10. (original) The circuit of claim 9 further comprising:

a control logic block, coupled to a match signal from the content addressable memory, generating a plurality of select signals, one coupled to each of the tristate buffer circuits.

Claim 11. (original) The circuit of claim 10 wherein based on the match signal, the control logic block generates select signals to enable one of the tristate buffers and disable others of the tristate buffers.

Claim 12. (original) The circuit of claim 10 wherein the control logic block comprises a state machine.

Claim 13. (currently amended) The circuit of claim 9 wherein there is one parallel data output ~~format~~ for each bit of the first parallel data output minus 1.

Claim 14. (original) The circuit of claim 8 wherein the shift register is divided into three portions, the first portion of the shift register is coupled to the deserializer, the second portion of the shift register is coupled to the first portion through a first multiplexer, and the third portion of the shift register is coupled to the second portion through a second multiplexer.

Claim 15. (currently amended) The circuit of claim 14 wherein the third portion ~~position~~ of the shift register is coupled to the first portion of the shift register through the second multiplexer.

Claim 16. (currently amended) The circuit of claim 14 wherein the second portion ~~position~~ of the shift register is coupled to the deserializer through the first multiplexer.

Claim 17. (original) The circuit of claim 8 wherein each row in the content addressable memory comprises a data pattern to be detected in the serial data input.

Claim 18. (original) The circuit of claim 8 wherein the content addressable memory has a number of rows equal to or greater than a number of bits of the first parallel data output.

Claim 19. (original) The circuit of claim 8 wherein the content addressable memory comprises a bit pattern comprising "1111," "0110," "0010," and "1000" in at least a number of rows that is equal to a number of bits of the first parallel data output.

Claim 20. (original) The circuit of claim 8 wherein the first parallel data output is 8, 10, 16, or 20 bits wide.

Claim 21. (original) A programmable logic integrated circuit comprising the circuit of claim 8.

Claim 22. (original) The circuit of claim 8 further comprising:

a plurality of parallel data output formats based on the first parallel data output; and

a selector circuit, coupled to each of the parallel data output formats and the first parallel data output, outputting one of the parallel data output formats as a second parallel data output based on an output from the content addressable memory.

Claim 23. (original) The circuit of claim 8 wherein the first parallel data output comprises 8 bits in a format bit 0, bit 1, bit 2, bit 3, bit 4, bit 5, bit 6, and bit 7, and the circuit further comprises:

a first parallel data output format comprising bit 1, bit 2, bit 3, bit 4, bit 5, bit 6, bit 7, and bit 0;

a second parallel data output format comprising bit 2, bit 3, bit 4, bit 5, bit 6, bit 7, bit 0, and bit 1; and

a third parallel data output format comprising bit 3, bit 4, bit 5, bit 6, bit 7, bit 0, bit 1 and bit 2;

a fourth parallel data output format comprising bit 4, bit 5, bit 6, bit 7, bit 0, bit 1, bit 2, and bit 3;

a fifth parallel data output format comprising bit 5, bit 6, bit 7, bit 0, bit 1, bit 2, bit 3, and bit 4;

a sixth parallel data output format comprising bit 6, bit 7, bit 0, bit 1, bit 2, bit 3, bit 4, and bit 5; and

a seventh parallel data output format comprising bit 7, bit 0, bit 1, bit 2, bit 3, bit 4, bit 5, and bit 6.

Claim 24. (previously presented) A method comprising:

deserializing an input serial data stream into a first parallel word;

generating a second parallel word from the first parallel word;

grouping the second parallel word into a plurality of data word subsets that overlap to include at least one common data bit;

generating a third parallel word from the first and second parallel word; and

detecting a frame alignment symbol within the third parallel word by comparing a bit pattern of the third parallel word to a plurality of frame alignment patterns stored in a content addressable memory.

Claim 25. (previously presented) The method of claim 24, further comprising selecting one of the subsets associated with a respective one of the frame alignment patterns that matches the frame alignment symbol.

Claim 26. (previously presented) The method of claim 24, wherein detecting the frame alignment symbol comprises detecting the frame alignment symbol within one clock cycle.

Claim 27. (previously presented) The method of claim 24, wherein grouping the second parallel word comprises outputting the second parallel word on a data bus that includes subsets of data lines that correspond to the data word subsets.